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Paper 10
Date: October 3, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MEDIATEK, INC.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC.,
Patent Owner.

IPR2024-00720
Patent 8,253,438 B2

Before KEN B. BARRETT, JOHN F. HORVATH, and ELIZABETH M. ROESEL, *Administrative Patent Judges.*

HORVATH, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background and Summary

MediaTek, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–19 ("the challenged claims") of U.S. Patent No. 8,253,438 B2 (Ex. 1001, "the '438 patent"). Paper 2 ("Pet."), 1. MOSAID Technologies Inc. ("Patent Owner") filed a Preliminary Response. Paper 8 ("Prelim. Resp."). We have jurisdiction and authority under 35 U.S.C. §§ 6, 314 and 37 C.F.R. § 42.4.

Upon consideration of the Petition and Preliminary Response, on the record before us, we find Petitioner has failed to demonstrate a reasonable likelihood that it would prevail in showing the unpatentability of any of the challenged claims. Accordingly, we decline to institute *inter partes* review.

B. Real Parties-in-Interest

Petitioner identifies itself and MediaTek USA, Inc. as real parties-in-interest. Pet., 92. Patent Owner identifies itself as the real party-in-interest. Paper 6, 1.

C. Related Matters

Petitioner and Patent Owner identify *MOSAID Techs. Inc. v. MediaTek, Inc.,* 2:23-cv-00129 (EDTX) (the "related litigation"), as a district court proceeding that can affect or be affected by this proceeding. Pet., 92; Paper 6, 1. Patent Owner also identifies *Conversant Intell. Prop. Mgmt.*, *Inc. v. Samsung Elec's.Co., Ltd.*, 2:15-cv-00281 (EDTX) as a district court proceeding that can affect or be affected by this proceeding. Paper 6, 1. We identify IPR2024-00598, -00600, -00718, -00719, and -00721 as Patent Office proceedings that can affect or be affected by this proceeding, as well as the following district court cases: *Mosaid Techs., Inc. v. Freescale Semiconductor, Inc.*, 6:11-cv-173 (EDTX), *Conversant Intell.*

Prop. Mgmt., *Inc. v. Xilinx, Inc.*, 6:12-cv-847 (EDTX), and *Conversant Intell. Prop. Mgmt.*, *Inc. v. STMicroelectronics, Inc.*, 6:12-cv-848 (EDTX).

D. The '438 Patent

The '438 patent is directed toward integrated circuits that include low leakage and data retention circuitry. Ex. 1001, 1:25–27. The patent explains that lowering the threshold voltage for CMOS[1] transistors increases performance but also increases leakage current and power consumption. *Id.* at 1:40–43. The patent then describes known methods of suppressing leakage current, including adding "sleep" transistors in series with logic gates that "act as a switch to turn on and off the logic gate[s]," and turning the sleep transistors "on" during logic gate operation and "off" when the logic gates are idle. *Id.* at 2:4–14.

The patent teaches dividing an integrated circuit into "power islands" so that "[p]ower consumption can then be controlled within the power island." *Id.* at 3:46–48. "A power island is any section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division." *Id.* at 3:62–65. Figure 2 of the patent, reproduced below, illustrates an integrated circuit (IC) divided into a plurality of power islands.

[1] Complementary Metal Oxide Semiconductor

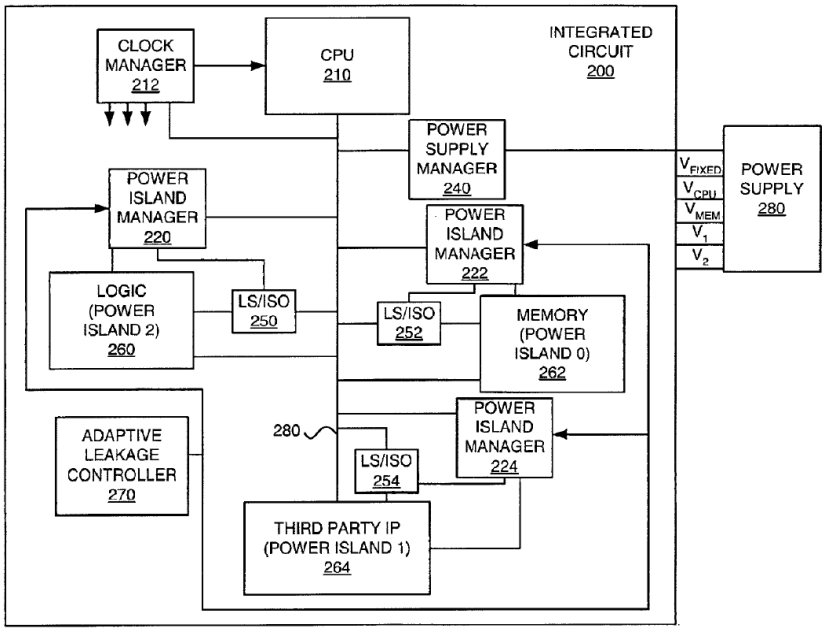


Figure 2 illustrates IC 200 divided into a plurality of components (e.g., logic 260, memory 262, third party IP 264) that are "power islands" because their power consumption is managed by power island managers 220, 222, and 224 in communication with adaptive leakage controller (ALC) 270. *Id.* at 2:60–61, 3:53–61. IC 200 includes other components (e.g., CPU 210, clock manager 212, power supply manager 240) that are not power islands because their power consumption is not managed. *Id.*

ALC 270 "provides control signals to compensate for process and temperature variations to provide the optimum voltage to be applied to sleep transistors in the power islands." *Id.* at 4:18–20. Power island managers 220, 222, 224 "are any circuitry, device or system configured to provide control signals to a power island to control power within the power island." *Id.* at 4:8–11. For example, they can be circuitry to "select a clock, change clock frequency, or modify the voltage within the power island to control the power consumption of the power island." *Id.* at 4:14–17.

E. Illustrative Claim

Claims 1 and 15 are independent, and claims 2–14 and 16–19 depend directly or indirectly from them, respectively. Ex. 1001, 13:10–14:43. Claim 1, which is illustrative of the challenged claims, is reproduced below.

> 1. An integrated circuit comprising:
>
> a plurality of power islands having associated power consumptions, each of the power islands including circuitries and sleep transistors in coupled relation with the circuitries, and the sleep transistors being included within the integrated circuit to facilitate reduction of power consumed by the circuitries;
>
> a power island manager configured to dynamically change the power consumptions based on needs and operation of the integrated circuit, the power island manager in communication with at least one of the power islands; and
>
> an adaptive leakage controller configured to control change of a variable voltage to be applied to the sleep transistors, and the power island manager configured to generate the variable voltage based on a control signal received from the adaptive leakage controller.

Id. at 13:10–26.

F. Evidence

Reference		Effective Date	Exhibit
Takahashi	US 2003/0025130 A1	Feb. 6, 2003	1004
Mizuno	US 2003/0102904 A1	June 5, 2003	1005
Schutz	US 5,440,520	Aug. 8, 1995	1007
Notani	US 6,556,071 B2	Apr. 29, 2003	1025

Petitioner also relies upon the Declaration of Paul Min, Ph.D. Ex.1003.

G. Asserted Grounds

Petitioner asserts the challenged claims are unpatentable on the following grounds:

Ground	Claims	35 U.S.C. §	References
1A	1–19	103	Takahashi
1B	7, 19	103	Takahashi, Schutz
1C	9, 15	103	Takahashi, Notani
2A	1–19	103	Mizuno
2B	9, 15	103	Mizuno, Notani

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner identifies a person of ordinary skill in the art ("POSITA") at the time of the invention as someone that would have had "at least a bachelor of science degree in electrical engineering, computer engineering, computer science, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components, or software for controlling electronic circuits or components, or equivalent, with additional education substituting for experience and vice-versa." Pet. 5 (citing Ex. 1003 ¶ 24). Patent Owner does not dispute this definition; nor does Patent Owner offer an alternative definition. Prelim. Resp. 1–68.

"[T]he level of skill in the art is a prism or lens through which a judge, jury, or the Board views the prior art and the claimed invention." *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). At this stage of the proceeding, we find Petitioner's assessment of the level of skill in the art to be reasonable and commensurate with the problems and solutions disclosed in the prior art. *See In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Accordingly, for purposes of this Decision, we adopt Petitioner's description as our own.

B. Claim Construction

In *inter partes* reviews, we interpret a claim "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2019). Under this standard, a claim is construed "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." *Id.* However, only claim terms which are in controversy need to be construed and only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

The parties dispute whether the terms "power island" and "based on the needs and operation of the integrated circuit" require construction. Petitioner submits that "no claim terms require a formal construction." Pet. 6. Patent Owner contends both terms require construction. Prelim. Resp. 5, 6, 14. Because our Decision does not depend on the construction of either term, we need not construe them. *Nidec Motor*, 868 F.3d at 1017.

C. Obviousness over Takahashi

Petitioner contends claims 1–19 are unpatentable as obvious over Takahashi. Pet. 6–37. Patent Owner contends Takahashi fails to teach or suggest "a plurality of power islands" and dynamically changing the power consumption of the power islands "based on needs and operation of the integrated circuit" as those terms are construed by Patent Owner. Prelim. Resp. 9, 10, 18–57.

On the record before us, we find Petitioner fails to demonstrate a reasonable likelihood of showing at least one of the challenged claims is unpatentable as obvious over Takahashi for the reasons discussed below.

1. Takahashi

Takahashi discloses "a semiconductor integrated circuit by which power consumption can be reduced by suppressing leakage current." Ex. 1004 ¶ 1. This is illustrated, for example, in Figure 16, which is reproduced below.

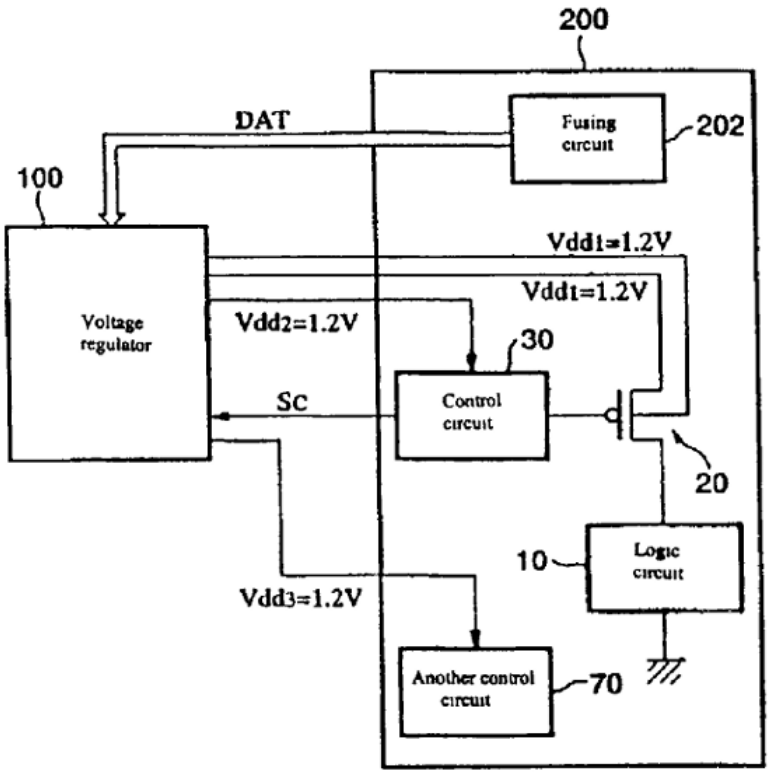


Figure 16 is a more detailed illustration of Figure 11 showing voltage control of individual circuits within device 200. *Id.* ¶¶ 97, 112, Fig. 11. Voltage regulator 100 supplies "multiple different levels of voltages V_{dd1}, V_{dd2}, and V_{dd3}" to different circuits in device 200 based on control data DAT provided by fusing circuit 202 and status control signal SC provided by control circuit 30. *Id.* ¶¶ 98–99, 113. Control data DAT is set by "cutting off a fuse provided in fusing circuit 202" and is used to select source voltages V_{dd1}, V_{dd2}, and V_{dd3} for transistors in different circuits in order to compensate for "variations during the production process." *Id.* ¶¶ 99–100.

Status control signal SC selects "awake" and "sleep" values for these voltages based on "the operating condition of the device." *Id.* ¶¶ 109–110.

As shown in Figure 4, logic circuit 10 can be an inverter consisting of pMOS[2] transistor MP1 and NMOS[3] transistor MN1, but can also be another type of logic circuit such as an AND gate, NAND gate, or OR gate. *Id.* ¶ 50, Fig. 4. Transistors MP1 and MN1 "are so-called low threshold MOS transistors having a threshold voltage . . . lower than that of a normal transistor." *Id.* Switching circuit 20 is a pMOS transistor MP0, and "supplies an operating current to logic circuit 10 during operation and suppresses the leakage current of the low threshold transistor[s] of logic circuit 10 during standby." *Id.* ¶ 51, Figs. 1, 4.

2. Claims 1–19

Independent claims 1 and 15 recite an integrated circuit that includes "a plurality of power islands having associated power consumptions, each of the power islands including circuitries and sleep transistors in coupled relation with the circuitries." Ex. 1001, 13:10–14 (the "power islands" limitation). Dependent claims 2–14 and 16–19 contain the same recitation by virtue of their dependency from claims 1 and 15, respectively. 35 U.S.C. § 112 ¶ 4 ("A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.").

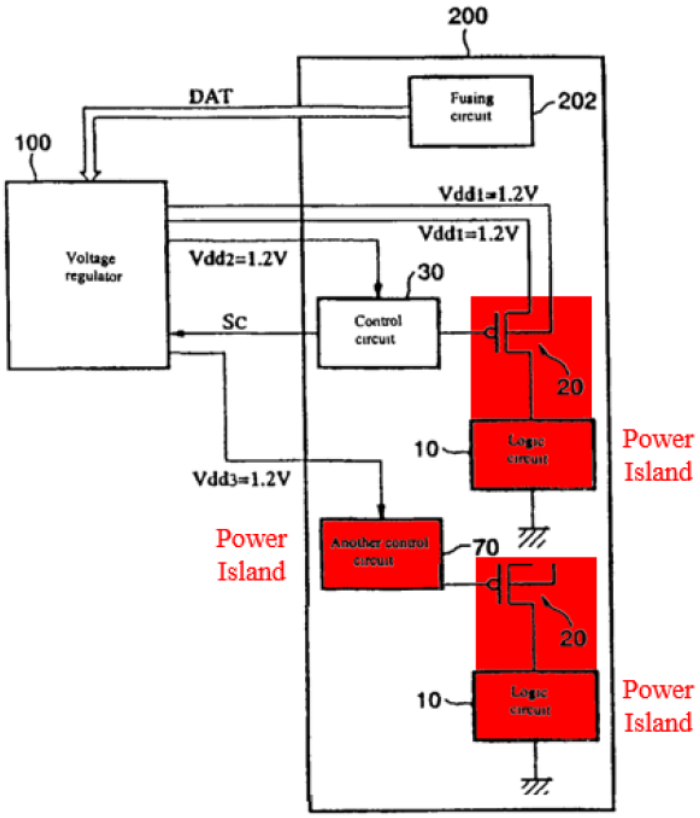
Petitioner argues the integrated circuits disclosed in Takahashi's Figures 1 or 16 teach or suggest this limitation. *See* Pet. 10–17 (citing Ex. 1004 ¶¶ 1, 3, 10, 45, 48, 50, 52, 54–59, 62, 78, 85, 90, 92, 110–116, 118, Figs. 1–17; Ex. 1003 ¶¶ 99–115). Specifically, Petitioner argues the

[2] P-type Metal Oxide Semiconductor
[3] N-type Metal Oxide Semiconductor

limitation is taught or suggested by Takahashi's unmodified Figure 16 or by a modification of Figure 1 or 16. *Id.*

Regarding unmodified Figure 16, Petitioner argues "Takahashi's logic circuit 10 (*i.e.*, circuitries) and 'switching circuit 20' (*i.e.*, sleep transistors) . . . comprise a power island." *Id.* at 11 (citing Ex. 1004 Figs. 1, 4–10, 16, 17; Ex. 1003 ¶ 102). Petitioner further argues a POSITA would have known that "Takahashi's 'control circuit 70' (*i.e.*, circuitries) would be coupled with a 'switching circuit 20' (*i.e.*, sleep transistors) and thus comprise another power island" or "would have found it obvious to include another 'switching circuit 20' . . . in 'control circuit 70' during standby to achieve . . . power savings." *Id.* at 12–13 (citing Ex. 1004 ¶¶ 110–116, Figs. 14–17; Ex. 1003 ¶¶ 103–104).

Regarding modifications to Figure 1 or 16, Petitioner argues "[a] POSITA would have found it obvious to incorporate multiple power islands as shown in Figure 10" into Takahashi's integrated circuit illustrated in Figure 1 or 16 in order "to provide additional functionality (*e.g.*, memory), and to control their individual power consumption." *Id.* at 14 (citing Ex. 1003 ¶ 108). More specifically, Petitioner argues that given Figure 10's disclosures, "[a] POSITA would have understood that a device can include more than one 'logic circuit' and been motivated to provide a 'switching circuit' (i.e., sleep transistor) for each to suppress leakage current." *Id.* at 14–15 (citing Ex. 1003 ¶¶ 108–110). The Petition includes an illustration of Figure 16, modified by Petitioner, which is reproduced below. *Id.* at 15.



The Figure above is Petitioner's modification of Takahashi's Figure 16. *Id.* In the modified figure, Petitioner identifies upper logic circuit 10 and switching circuit 20 as a "power island" (shown in red). *Id.* Petitioner modifies Figure 16 by adding lower logic circuit 10 and switching circuit 20, which Petitioner identifies as another "power island." *Id.*

Petitioner's contentions and mappings, which identify as power islands control circuit 70 coupled to *single* switching circuit 20 and/or logic circuit 10 coupled to *single* switching circuit 20, fail to demonstrate how Takahashi teaches or suggests the power islands limitation, which expressly requires each power island to include plural sleep transistors. *Compare* Pet. 11–13 (identifying logic circuit 10 and switching circuit 20 as a power island and control circuit 70 coupled to switching circuit 20 as a power island),

with Ex. 1001, 13:11–14, 14:20–25 (claims 1 and 15 requiring "each of the power islands [to] include[e] circuitries and [plural] sleep *transistors*").

To the extent Petitioner contends switching circuit 20 comprises multiple transistors (*see, e.g.,* Pet. 11–13, in which Petitioner parenthetically characterizes switching circuit 20 as "sleep transistors"), we disagree. Switching circuit 20 is illustrated and described throughout Takahashi, and is consistently illustrated and described as a *single* pMOS transistor. Ex. 1004 ¶¶ 51, 52, 70, 77, 79, 82, 84, 113, 116, Figs. 1, 4–9, 16, 17.

Accordingly, for this reason and on the record before us, we find Petitioner fails to demonstrate a reasonable likelihood of showing any of claims 1–19 unpatentable over Takahashi.

D. Obviousness over Takahashi, Schutz or Takahashi, Notani

Petitioner contends claims 7 and 19 are obvious over Takahashi and Schutz and claims 9 and 15 are obvious over Takahashi and Notani. Pet. 37–51. However, Petitioner relies solely on Takahashi to teach the power islands limitation in these claims. *Id.* Accordingly, for the reasons explained above, Petitioner fails to demonstrate a reasonable likelihood of showing claims 7 and 19 are unpatentable as obvious over Takahashi and Schutz or that claims 9 and 15 are unpatentable as obvious over Takahashi and Notani.

E. Obviousness over Mizuno

Petitioner contends claims 1–19 are unpatentable as obvious over Mizuno. Pet. 62–96. Patent Owner contends Mizuno fails to teach or suggest "a plurality of power islands" and dynamically changing the power consumption of the power islands "based on needs and operation of the integrated circuit" as those terms are construed by Patent Owner. Prelim. Resp. 9, 10, 57–65.

On the record before us, we find Petitioner fails to demonstrate a reasonable likelihood of showing at least one of the challenged claims is unpatentable as obvious over Mizuno for the reasons discussed below.

1. Mizuno

Mizuno discloses "a semiconductor integrated circuit device with excellent high speed and low power operation characteristics." Ex. 1005 ¶ 1. This is illustrated, for example, in Figure 1, which is reproduced below.

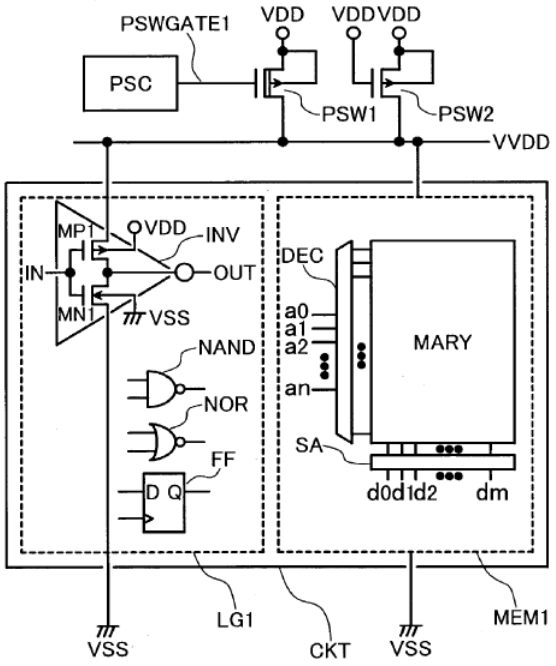


Figure 1 "is a circuit diagram showing the basic structure of the invention." *Id.* ¶ 53. An integrated circuit consists of circuit CKT (including logic LG1 and memory MEM1), power switch controller PSC, power switch PSW1, and current source PSW2. *Id.* ¶¶ 53, 54. Power switch controller PSC "controls the on and off operation of the power switch PSW1" and the "current flow in the power supply VDD and the virtual power line VVDD." *Id.* Current source PSW2 "limits the current flowing to the virtual power line VVDD from the power supply VDD." *Id.* The "current supplied to the circuit block [CKT] during operation is mainly supplied from the

power switch PS[W]l; and the current supplied to the circuit block during standby operation is mainly supplied [from] the current source PSW2." *Id.* The standby current is "smaller than the leakage current flowing in the circuit block CKT during operation." *Id.* ¶ 59.

Power switch controller PSC is controlled by power controlling circuit PMG as illustrated in Figure 22, which is reproduced below.

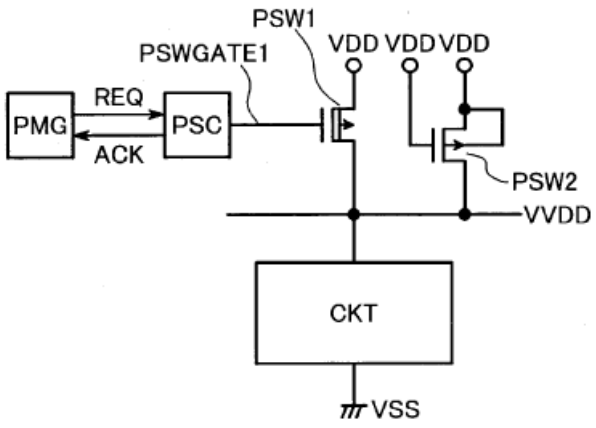


Figure 22 illustrates "the interface for the power switch controller PSC," which "controls the power switch PSW1 and current source PSW2 . . . by means of a power controlling circuit PMG." *Id.* ¶ 93. Through a request (REQ) and acknowledge (ACK) handshake, "the power controlling circuit PMG and the power switch controller PSC . . . controls the on/off operation of the power switch PSW1 and controls the state of the circuit block [CKT]." *Id.* Setting REQ high "turns on the power switch PSW1 and controls the circuit block CKT in the operation state." *Id.* Setting REQ low turns off PSW1 "and the circuit block is controlled to the standby state." *Id.*

Mizuno also discloses separately controlling the power consumption of a plurality of circuits in an integrated circuit in Figure 35, which is reproduced below.

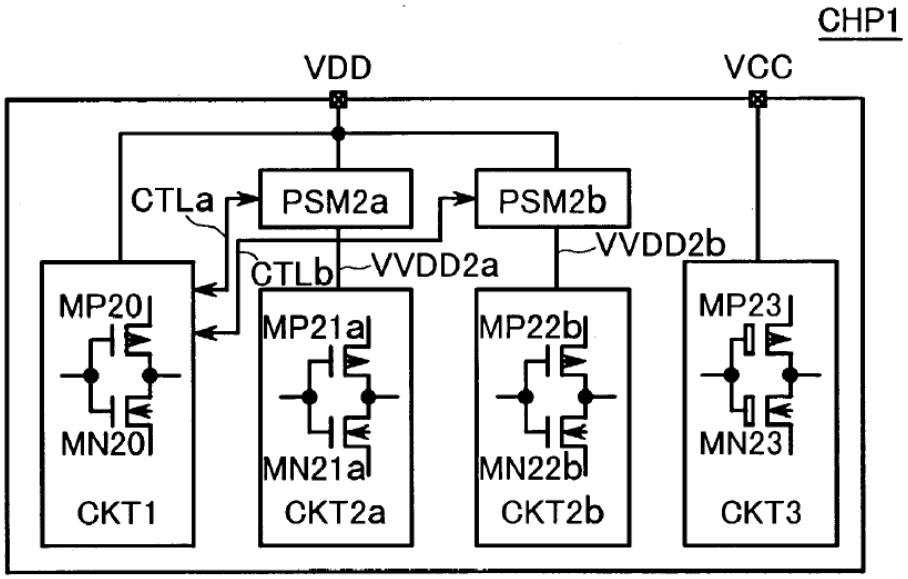


Figure 35 is a block circuit diagram of the chip CHP1 structure." *Id.* ¶ 121. Circuit block CKT1 is "supplied with power directly from a power supply VDD and not by way of [a] leakage reduction circuit" in order to receive a constant supply of power to "control the leakage reduction circuits PSM2a and PSM2b." *Id.* Circuit blocks CKT2a and CKT2b, by contrast, are "supplied with power from the current supply VDD by way of the leakage reduction circuits PSM2a and PSM2b." *Id.* Control lines CTLa and CTLb "are leakage control lines of the leakage reduction circuit . . . and [are] equivalent to the request line REQ and response link ACK of FIG. 22." *Id.* Mizuno discloses that "[b]y establishing multiple leakage control circuits as in FIG. 35, and controlling the leakage current of circuits grouped in multiple circuits integrated onto the chip, the leakage current of the overall chip can be efficiently reduced." *Id.* ¶ 122.

2. Claims 1–19

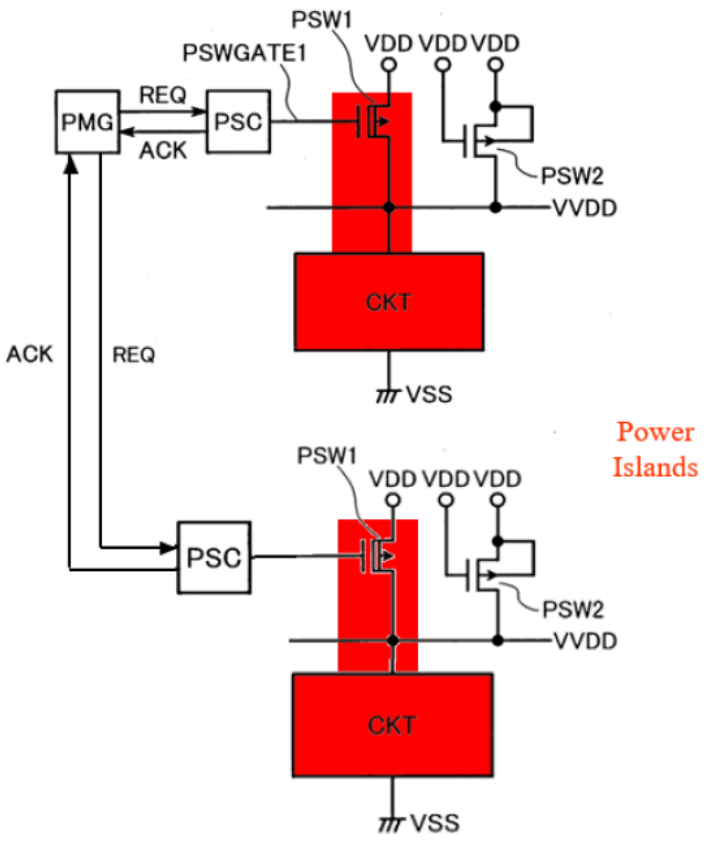
Independent claims 1 and 15 recite an integrated circuit that includes "a plurality of power islands having associated power consumptions, each of the power islands including circuitries and sleep transistors in coupled

relation with the circuitries." Ex. 1001, 13:10–14 (the "power islands" limitation). Dependent claims 2–14 and 16–19 contain the same recitation by virtue of their dependency from claims 1 and 15, respectively. 35 U.S.C. § 112 ¶ 4 ("A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.").

Petitioner argues the integrated circuit disclosed in Mizuno's first embodiment, particularly as illustrated in Figure 22, teaches or suggests this limitation. *See* Pet. 54–61 (citing Ex. 1005 ¶¶ 52–107, 121–133, Figs. 1–30, 35–40; Ex. 1003 ¶¶ 294–318). Specifically, Petitioner argues the limitation is taught or suggested by modifying Figure 22 based on the teachings of Figure 35. *Id.*

Regarding unmodified Figure 22, Petitioner argues "Mizuno's 'circuit block CKT,' . . . coupled to a power switch PSW1, comprises a power island." *Id.* at 55–56 (citing Ex. 1005 ¶¶ 53, 54, Figs. 1, 22; Ex. 1003 ¶¶ 296, 297. Petitioner argues Mizuno's Figure 35 illustrates a third embodiment "of an integrated circuit having multiple 'circuit blocks' that are power islands." *Id.* at 58 (citing Ex. 1005 ¶¶ 121–133, Fig. 35; Ex. 1003 ¶¶ 307–315). Therefore, Petitioner argues, a POSITA would have found it obvious "to include multiple power islands in Mizuno's 'first embodiment' (FIGS. 1–30) . . . based at least on Mizuno's disclosures with respect to its related 'third embodiment' (FIGS. 35–40)." *Id.* at 59 (citing Ex. 1003 ¶¶ 316–317).

Petitioner illustrates its contentions with a modified version of Figure 22, which is reproduced below. *Id.* at 59.



The Figure above is Petitioner's modified version of Mizuno's Figure 22. Petitioner identifies upper transistor PSW1 and circuitry CKT as a "power island" (shown in red) and modifies Figure 22 by adding lower transistor PSW1 and circuitry CKT, which Petitioner identifies as another "power island." *Id.*

Petitioner's contentions and mappings, which identify as a power island circuit CKT coupled to a *single* transistor PSW1, fail to demonstrate how Mizuno teaches or suggests the power islands limitation, which expressly requires each power island to have multiple sleep transistors. *Compare* Pet. 55–56 (identifying Figure 22's circuit block CKT and *single* power switch PSW1 as a power island), *with* Ex. 1001, 13:11–14, 14:20–25

(claims 1 and 15 requiring "each of the power islands [to] include[e] circuitries and [plural] sleep *transistors*").

Accordingly, for this reason and on the record before us, we find Petitioner fails to demonstrate a reasonable likelihood of showing any of claims 1–19 unpatentable as obvious over Mizuno.

F. Obviousness over Mizuno, Notani

Petitioner contends claims 9 and 15 are obvious over Mizuno and Notani. Pet. 85–89. However, Petitioner relies solely on Mizuno to teach the power islands limitations in these claims. *Id.* Accordingly, for the reasons explained above, Petitioner fails to demonstrate a reasonable likelihood of showing claims 9 and 15 are unpatentable as obvious over Mizuno and Notani.

III. CONCLUSION

We have reviewed the Petition and Patent Owner's Preliminary Response, and have considered all of the evidence and arguments presented by Petitioner and Patent Owner. We find, on the record before us, Petitioner has failed to demonstrate a reasonable likelihood of showing any of the challenged claims are unpatentable. Accordingly, we decline to institute *inter partes* review.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314, the Petition to institute *inter partes* review is denied.

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